

Appendix A. FFT Core Options

Table A.1: Xilinx LogiCore FFT Options and Setup

Option	Explanation	Setup	Reasoning
<i>Component Name</i>	Name of the core to be generated	FFT_block	Similar name to other stages/blocks in the system
<i>Number of Channels</i>	Number of I/O channels (only available for Radix-2-Lite)	2	Require two channels to pass in signals A and B
<i>Transform Length</i>	Point size of the transform, all powers of two from 8 to 65536	$2048 = 2^{11}$	Due to the $\sim 2kHz$ sampling frequency
<i>Implementation Options</i>	Choose an architecture option outlined in Section 4.2.2.3	Radix-2-Lite	Low resources required, and capable of multichannel
<i>Transform Length Options</i>	Can select to allow the transform length to be altered at run time	No	The transform length has no need to change
<i>Precision Options</i>	Input data width and phase factor	14	The ADC produces a 14-bit output
<i>Optional Pins</i>	Ability to enable extra options at the cost of resource	None	Minimise resources used
<i>Scaling Options</i>	Allow for the data in the block to be scaled by shifting bits	Scaled	Whilst not completely required, this option was left in should it be discovered that scaling was required
<i>Rounding Modes</i>	The least significant bit in the output of the butterfly needs to be trimmed	Convergent Rounding	Avoids the DC bias that would be introduced by Truncation
<i>Output Ordering</i>	Bits can be presented in natural order or bit-reversed order	Bit Reversed Order	Minimises overall transform time
<i>Memory Options</i>	Select whether Block RAM or Distributed RAM will be used	Block RAM	Minimise resources used
<i>Optimize Options</i>	Only available for Virtex FPGA boards, not the Spartan 3E	n/a	n/a